Amendments to the Specification

In the Abstract, please amend as shown.

~~A circuit under test (24) has a scan chain comprising flip-flop cells (10a-c) with inputs and outputs operationally connected to the logic circuits (12). Different clock domains each contain a respective part of the flip-flop cells (10a-c) that are clocked by a respective domain clock signal(CLKa, CLKb, CLKc). A set of test input patterns is selected, each with an associated combination of domain clock signals that will be selectively enabled to capture a response to the test pattern. The set contains particular test patterns that have the properties that (a) the response captured by a timing sensitive flip-flop cell (10a-c) in a first clock domain is used to detect a fault, (b) the timing sensitive flip-flop cell (10a-c) receives data dependent on data from a source flip-flop cell (10a-c) that belongs to a second clock domain different from the first clock domain, and (c) the combination of selectively enabled domain clock signals associated with the particular test pattern comprises the clocks of both the first and second domain. These particular test patterns also have the property that the data value in the source flip-flop cell (10a-c) is identical to a response value captured by the source flip-flop cell (10a-c) for the particular test pattern. Preferably, the set of test patterns is generated for a virtual circuit obtained by additional logic circuits (30, 40, 42) are added to the design of real the circuit under test. The additional logic circuits (30, 40, 42) are designed to selectively enable a dependence of an input signal of the timing sensitive flip-flop cell (10a-c) on data from the source flip-flop cell (10a-c) when the input and output signals of the source flip-flop cell (10a-c) are identical and the second domain clock is enabled.~~

~~Fig. 3~~

Consistent with an example embodiment, the amount of time required for testing circuits that contain a plurality of different clock domains is reduced. According to the embodiment, during selection of the input test pattern to test logic circuits between a timing sensitive flip-flop in a first clock domain that captures a response that depends on

test data in a source flip-flop in a second, different clock domain, account is taken of whether the data in the first flip-flop will change value if it is clocked when the response is captured. If not, it may be assumed that uncertainty about the timing relationship of different clock domains does not introduce uncertainty with respect to the data from the timing sensitive flip-flop, so that the response data at the second flip-flop can be treated as reliable

In the Specification, page 3, lines 15-25, please amend as shown.

A circuit testing system according to an embodiment of the invention is set forth. ~~the invention is set forth in Claim 1.~~ There is circuit testing system, for testing a circuit under test with logic circuits and a scan chain comprising flip-flop cells with inputs and outputs operationally connected to the logic circuits. The circuit under test includes a plurality of clock domains, each containing a respective part of the flip-flop cells that are clocked by a respective domain clock signal. The circuit testing system comprises a test controller arranged to switch the circuit under test to a test mode wherein the test controller supplies successive test input patterns through the scan chain. Each test input pattern is associated with a respective combination of domain clock signals that are selectively enabled to capture a response of the logic circuits to the test input pattern into flip-flop cells of the scan chain; the test controller uses the captured response from at least part of the flip-flop cells to detect faults in the circuit under test. A test pattern selector is arranged to select a set of test input patterns and the associated combinations of domain clock signals for use by the test controller, wherein a particular test pattern in the selected set that has properties which include, the response to the particular test pattern captured by a timing sensitive flip-flop cell in a first clock domain is used to detect a fault, the timing sensitive flip-flop cell receives data dependent on data from a source flip-flop cell that belongs to a second clock domain different from the first clock domain, the combination of selectively enabled domain clock signals associated with the particular test pattern comprises the clocks of both the first and second domain, and also has the further property that the data value in the source flip-flop cell is identical to a response value captured by the source flip-flop cell for the particular test pattern.

_____According to the invention, during selection of the input test pattern to test logic circuits between a timing sensitive flip-flop in a first clock domain that captures a response that depends on test data in a source flip-flop in a second, different clock domain, account is taken of whether the data in the first flip-flop will change value if it is clocked when the response is captured. If not, it may be assumed that uncertainty about the timing relationship of different clock domains does not introduce uncertainty with respect to the data from the timing sensitive flip-flop, so that the response data at the second flip-flop can be treated as reliable.